**DIGITAL ELECTRONICS**

**PRACTICAL FILE**

**SIMULATED CIRCUITS RECORD**

SUBMITTED BY:

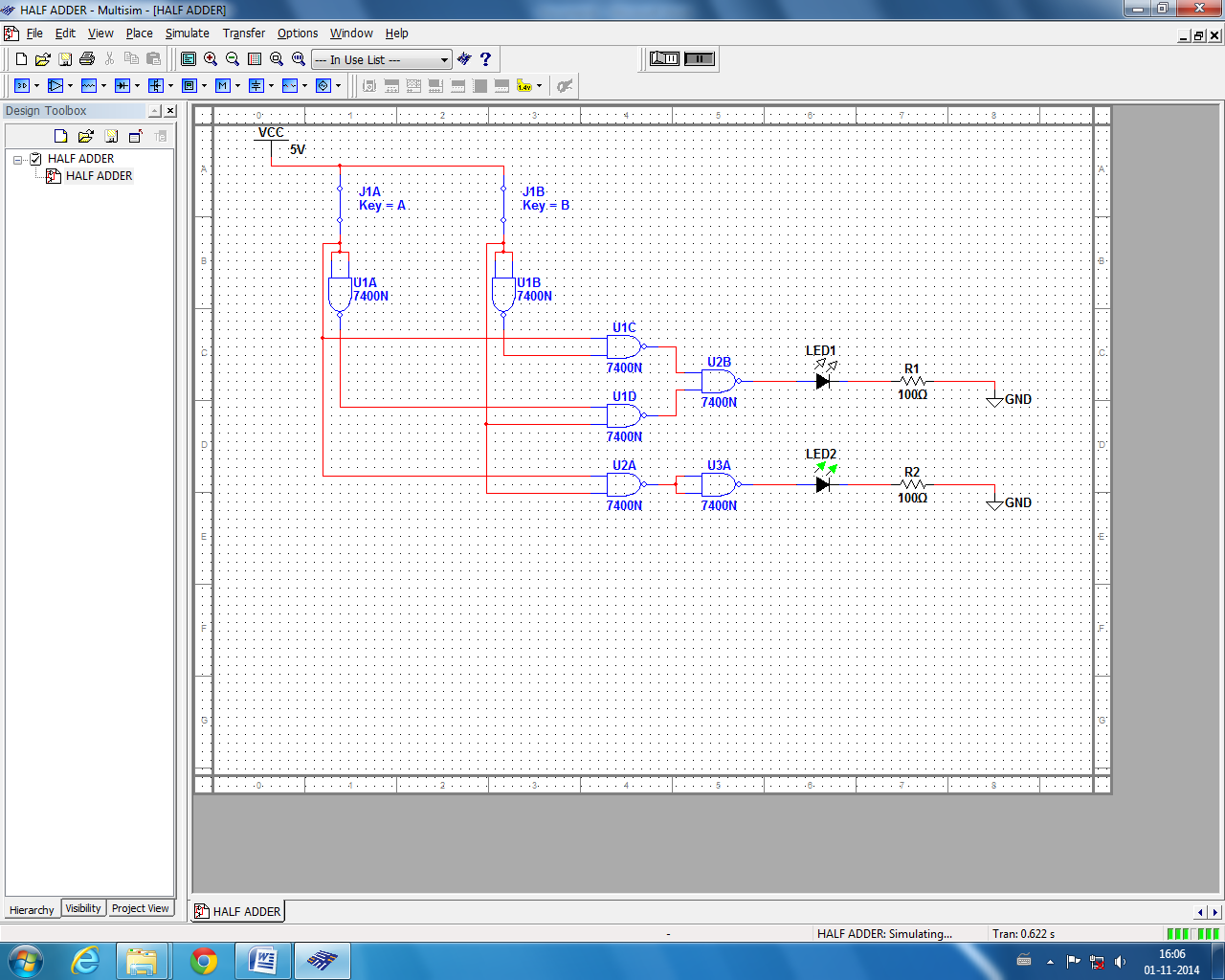
**DEEPTI SHARMA**

**2014315**

BSc(Hons).COMPUTER SCIENCE

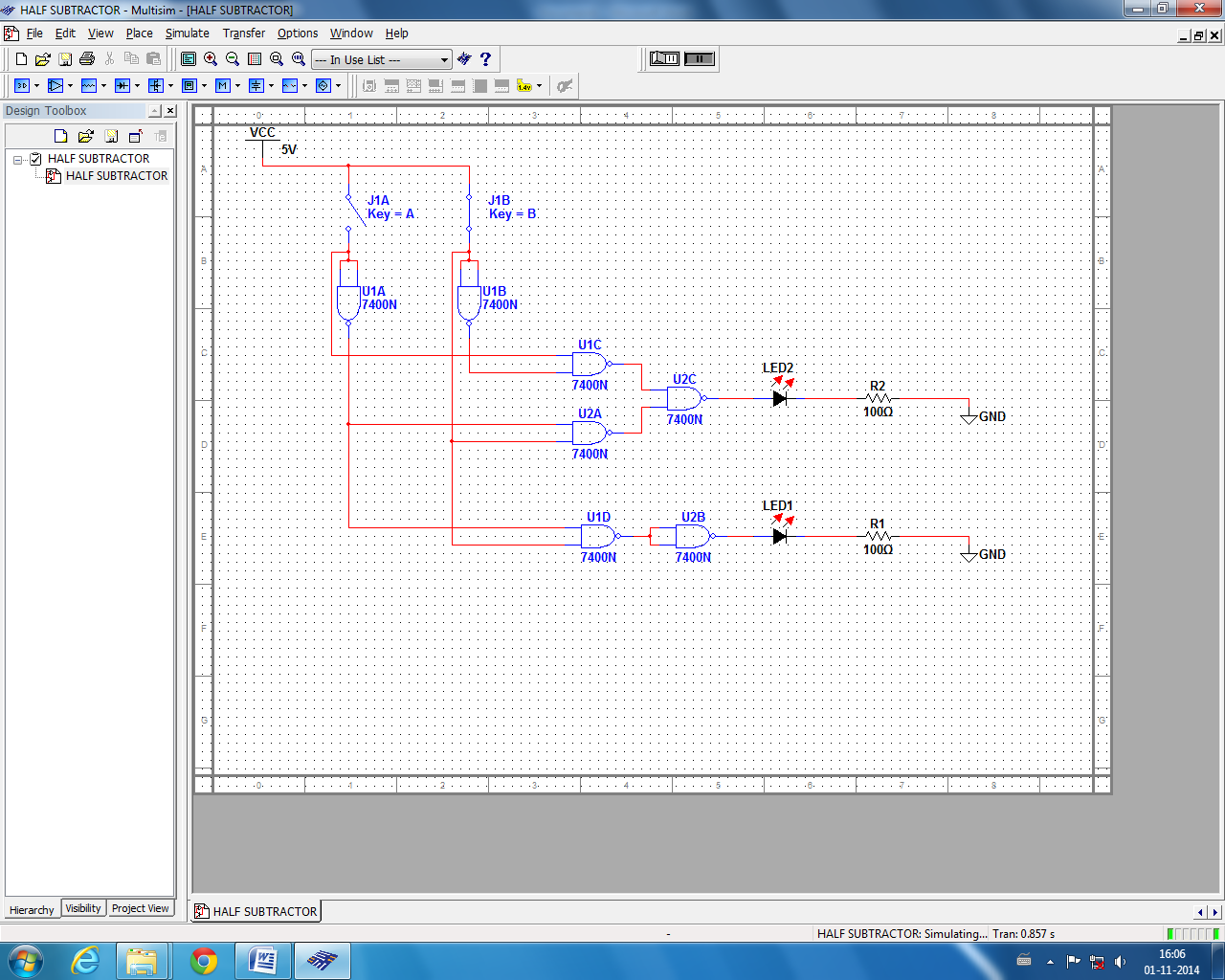
1st Year, Semester: 1

**Experiment: 1**

**Aim:**  To implement half adder using NAND gates.

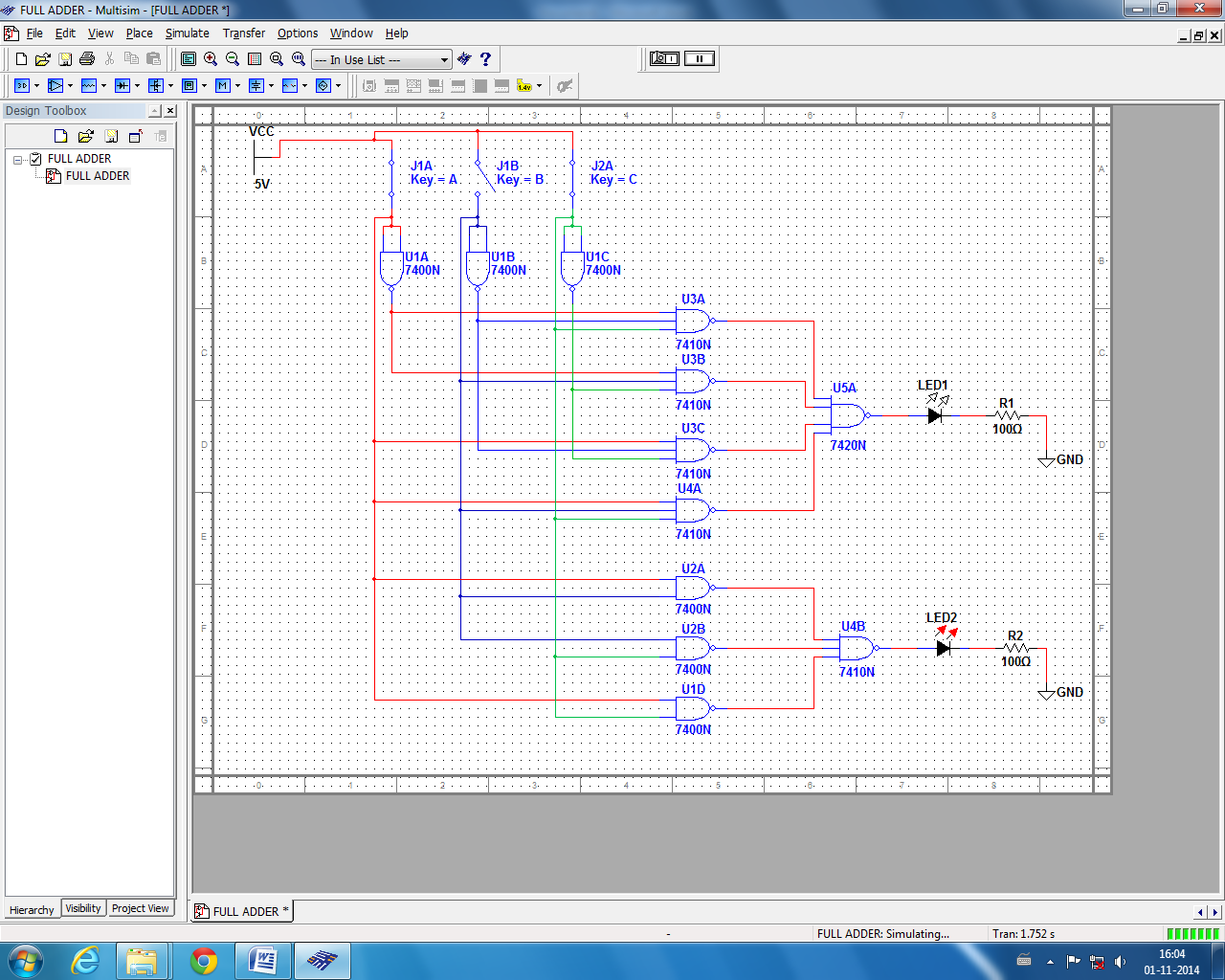
**Experiment: 2**

**Aim:**  To implement half subtractor using NAND gates.



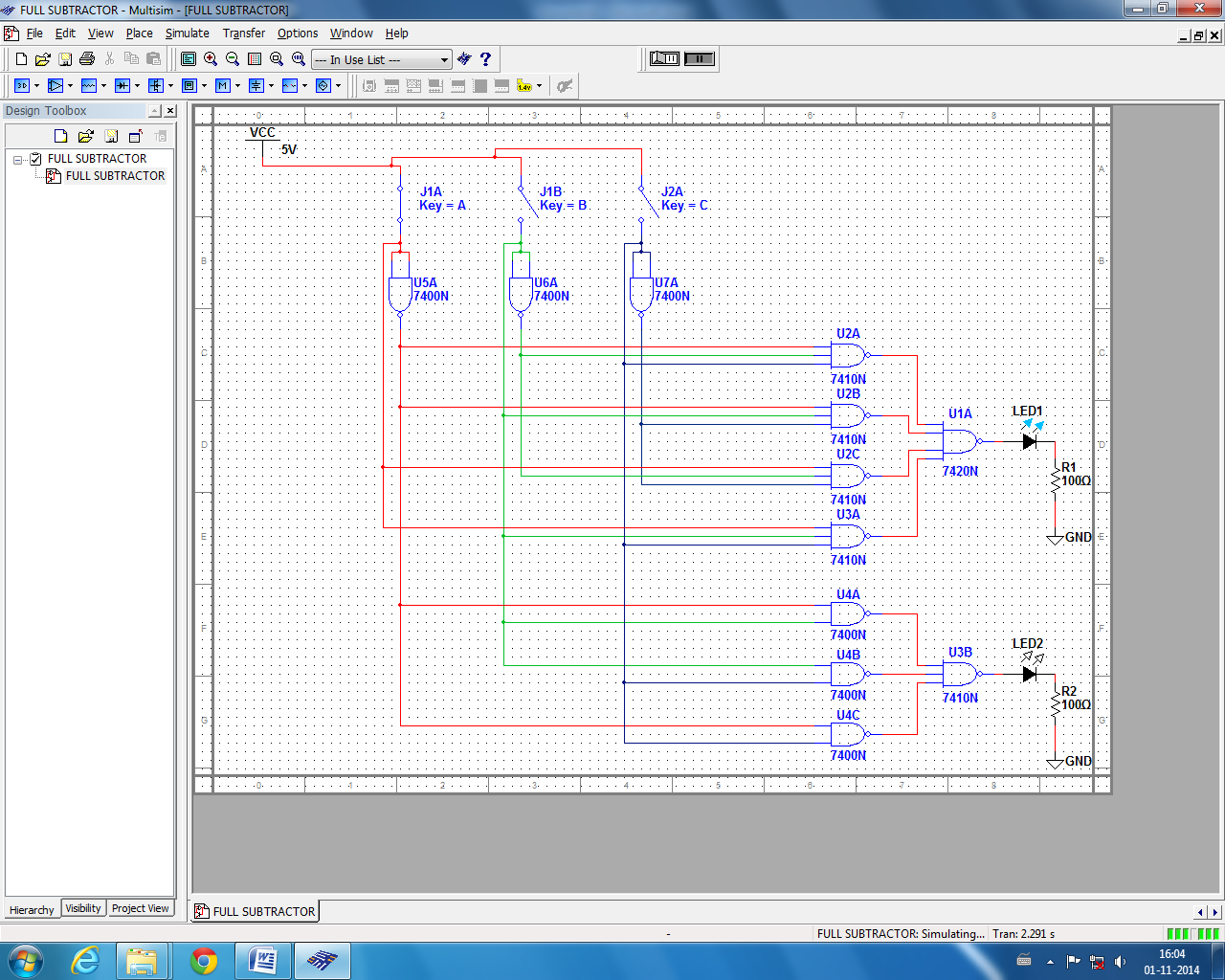
**Experiment: 3**

**Aim:**  To implement full adder using NAND gates.



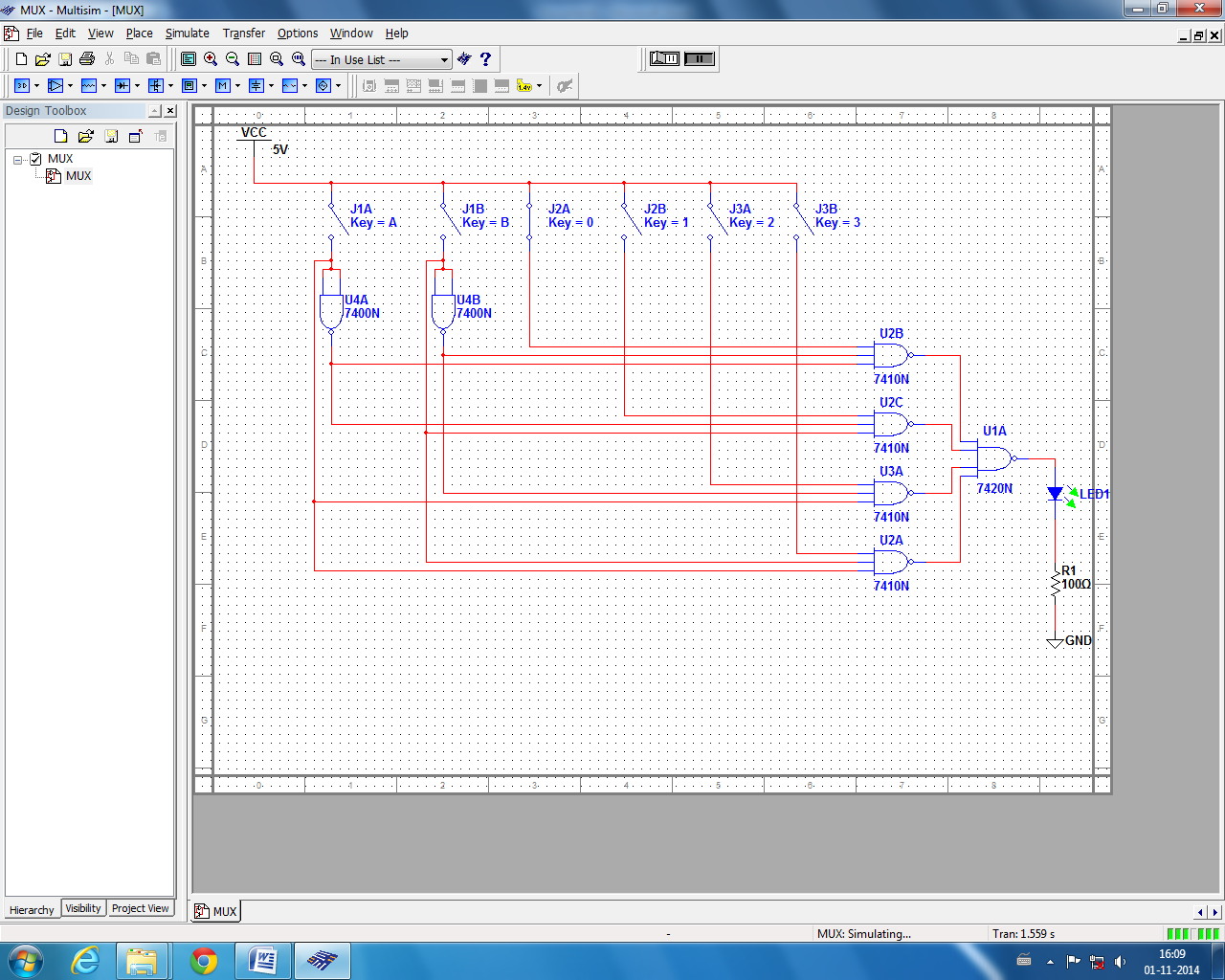
**Experiment: 4**

**Aim:**  To implement full subtractor using NAND gates.



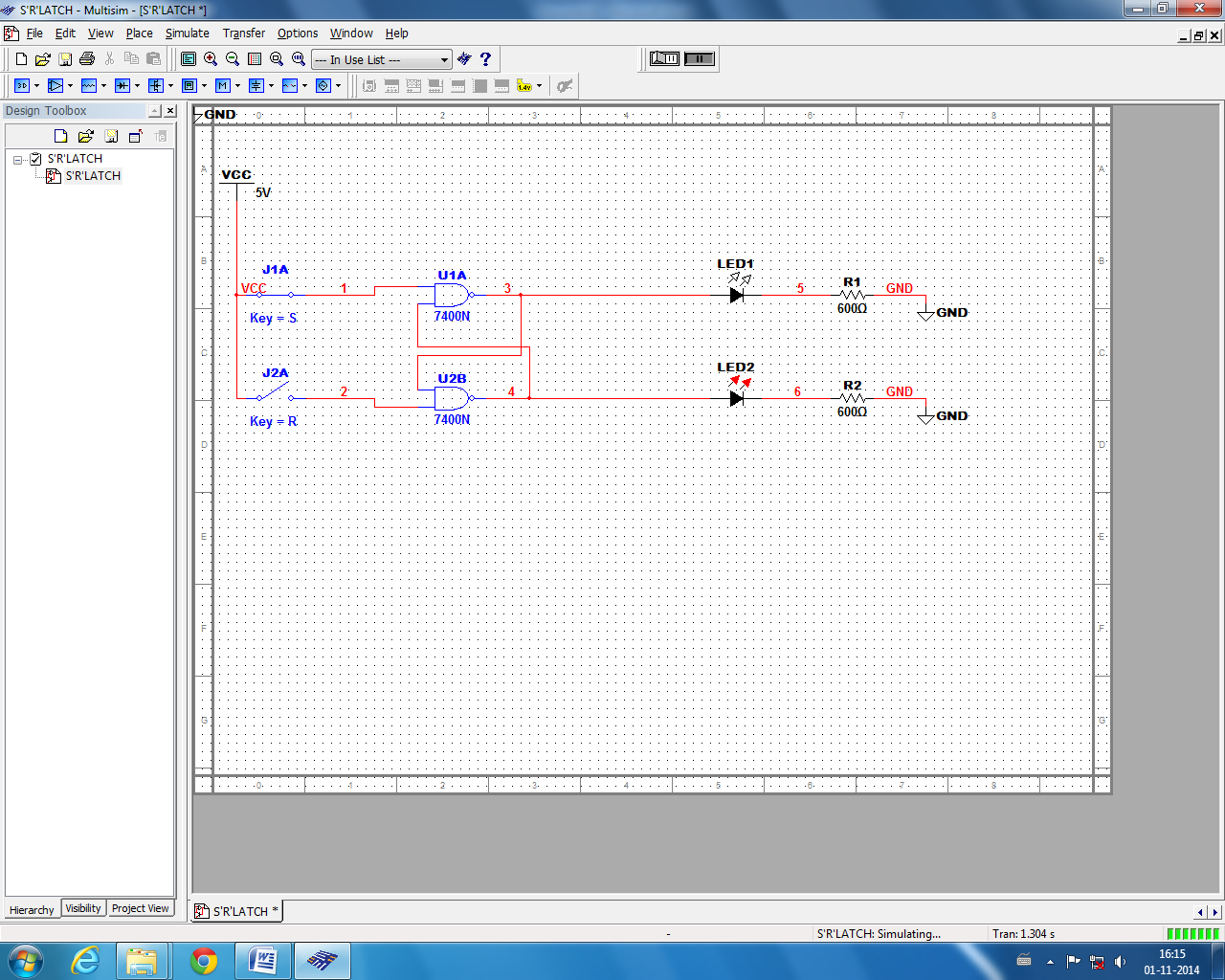
**Experiment: 5**

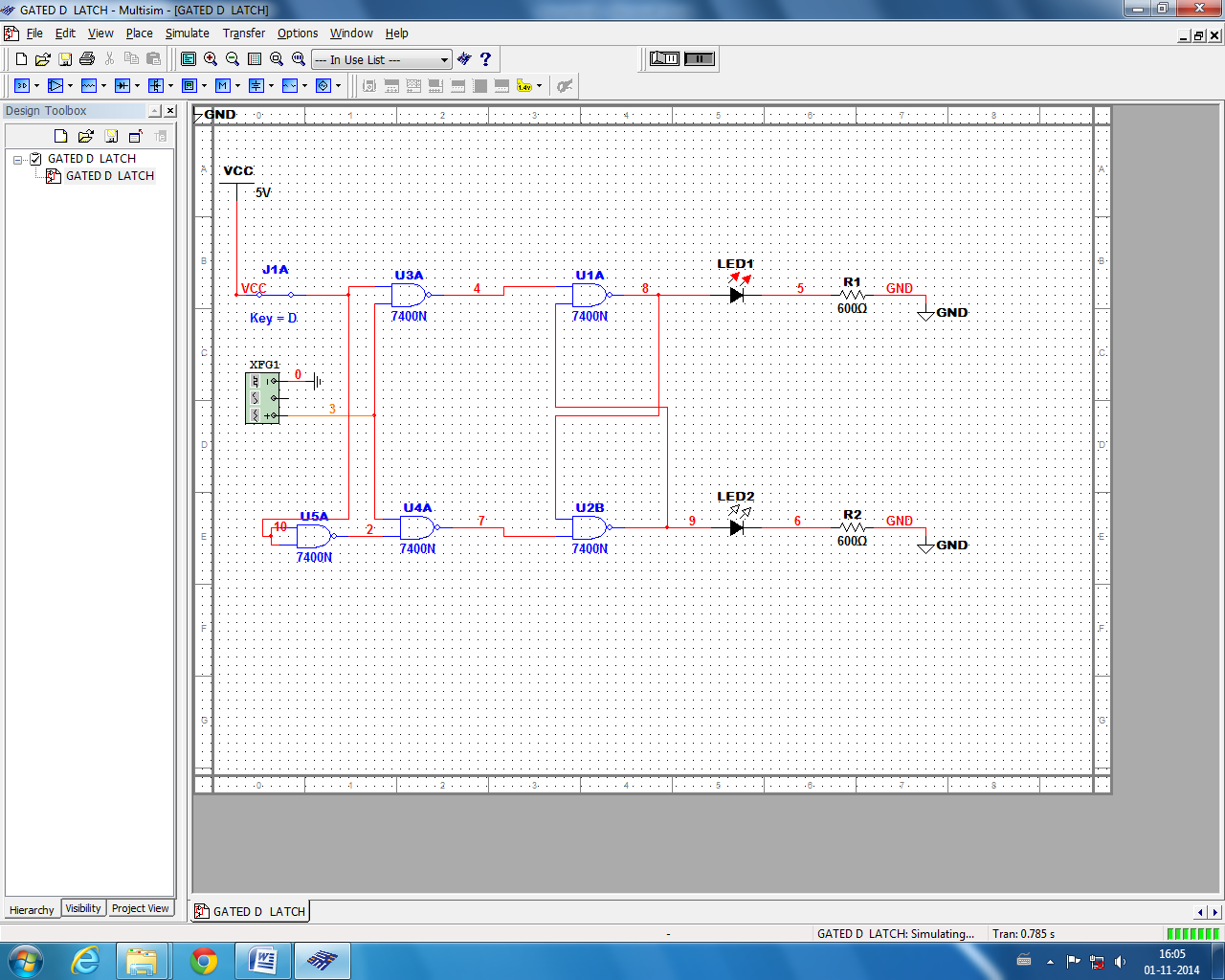
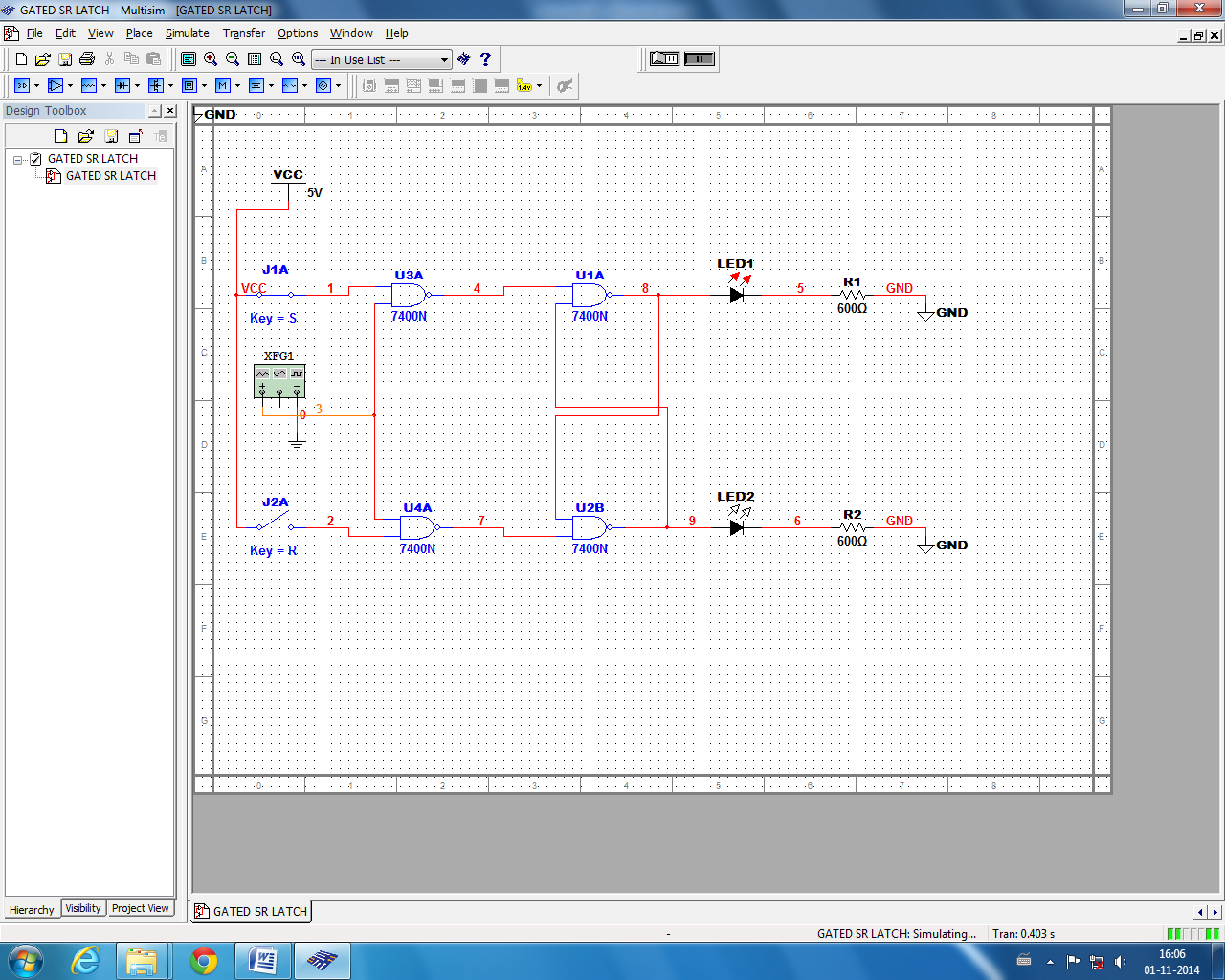
**Aim:**  To implement 4x1 Multiplexer.



**Experiment: 6**

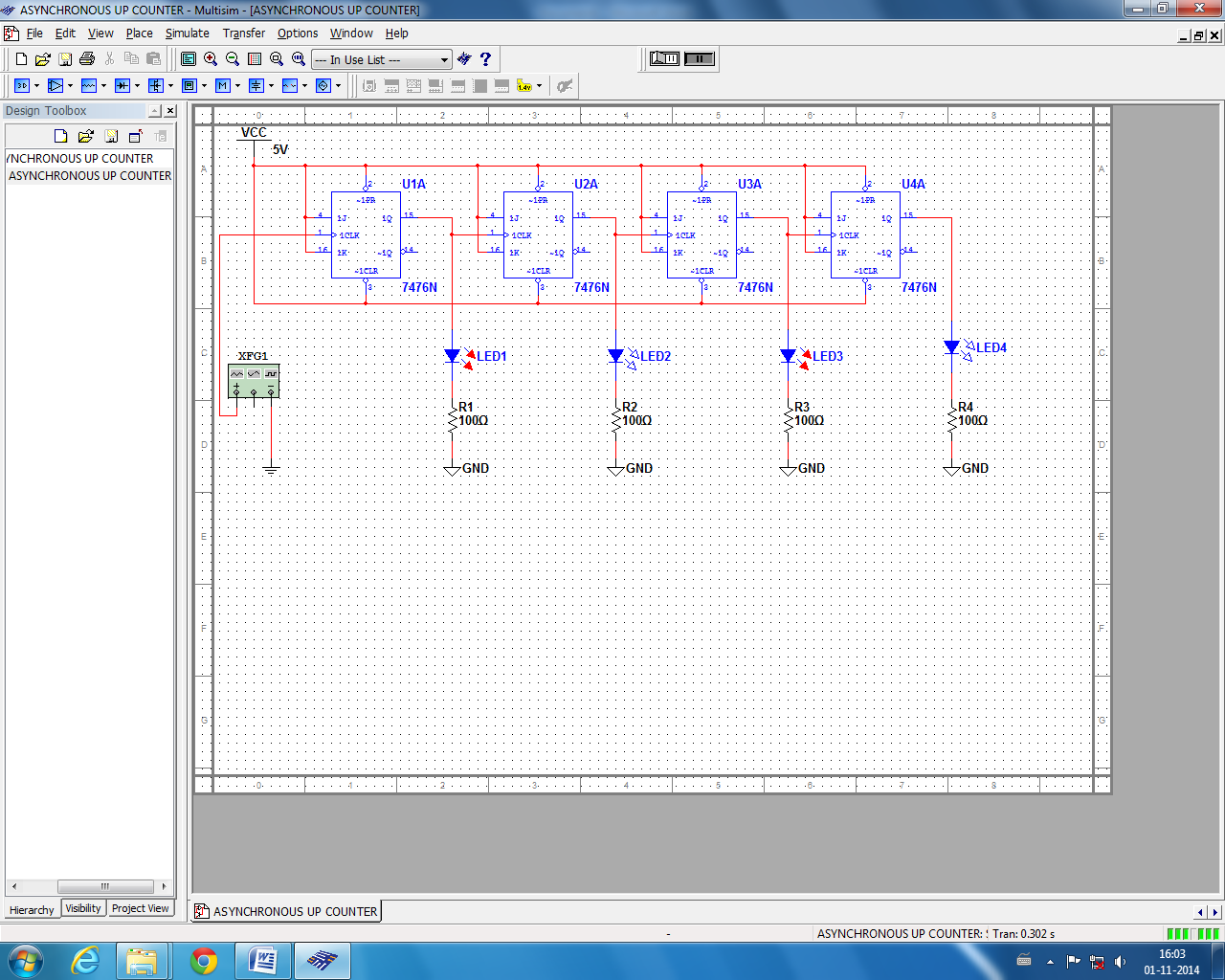
**Aim:**  To design and build a flip–flop circuit using elementary gates.

1. S’R’ LATCH:
2. Gated SR LATCH:



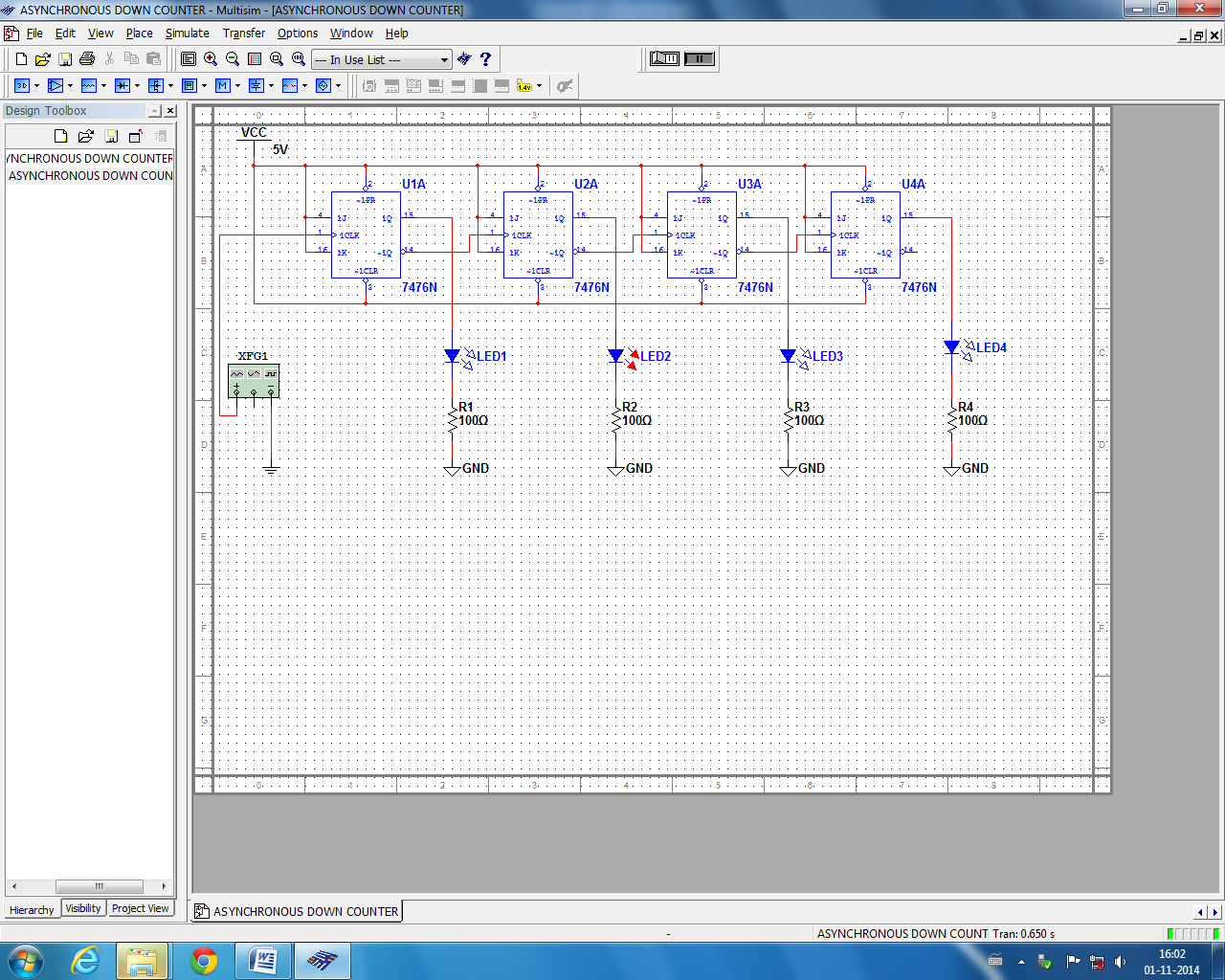
3. Gated D LATCH:

**Experiment: 6**

**Aim:**  To design an Asynchronous 4 BIT UP counter using JK flip flop.

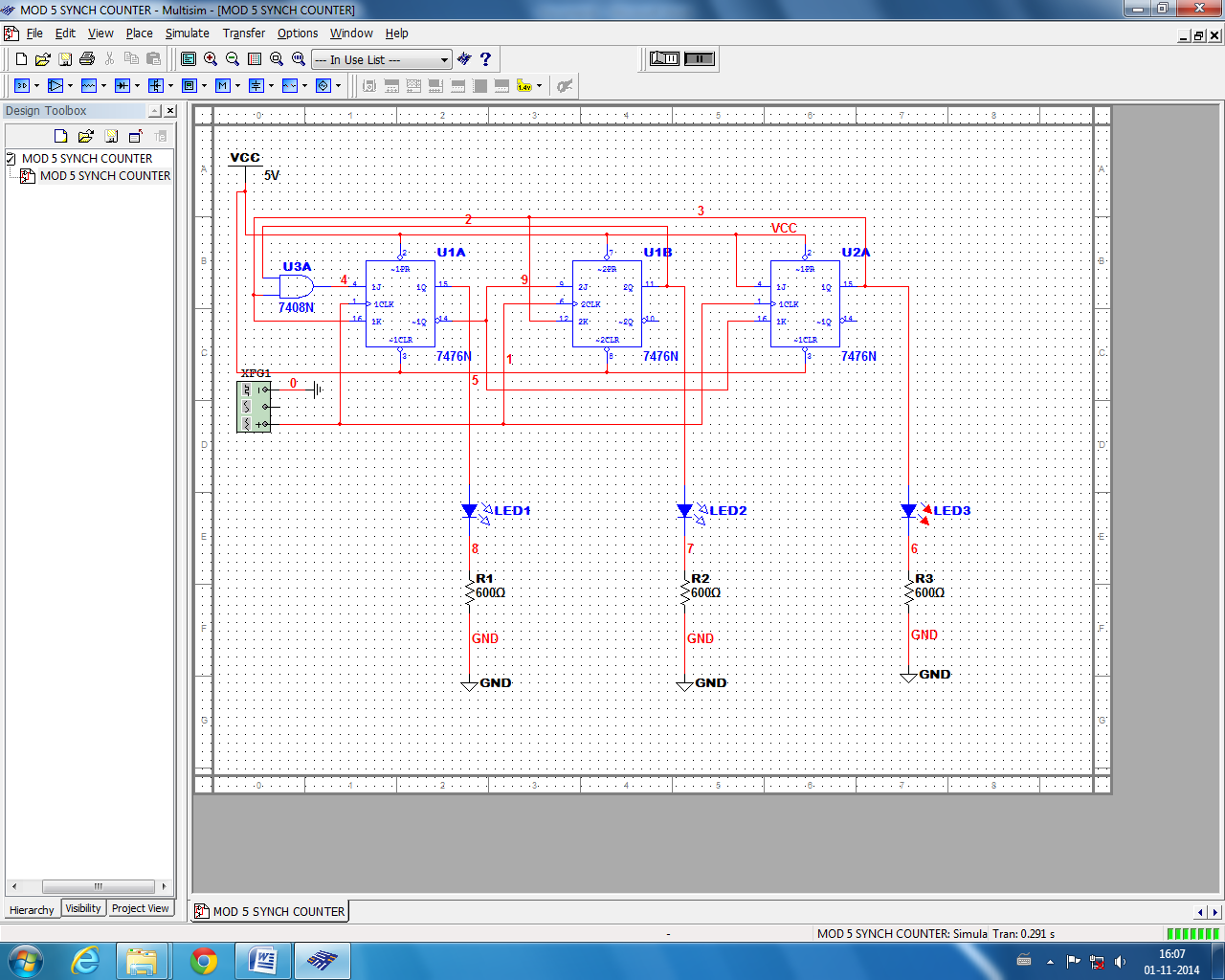
**Experiment: 7**

**Aim:**  To design an Asynchronous 4 BIT DOWN counter using JK flip flop.

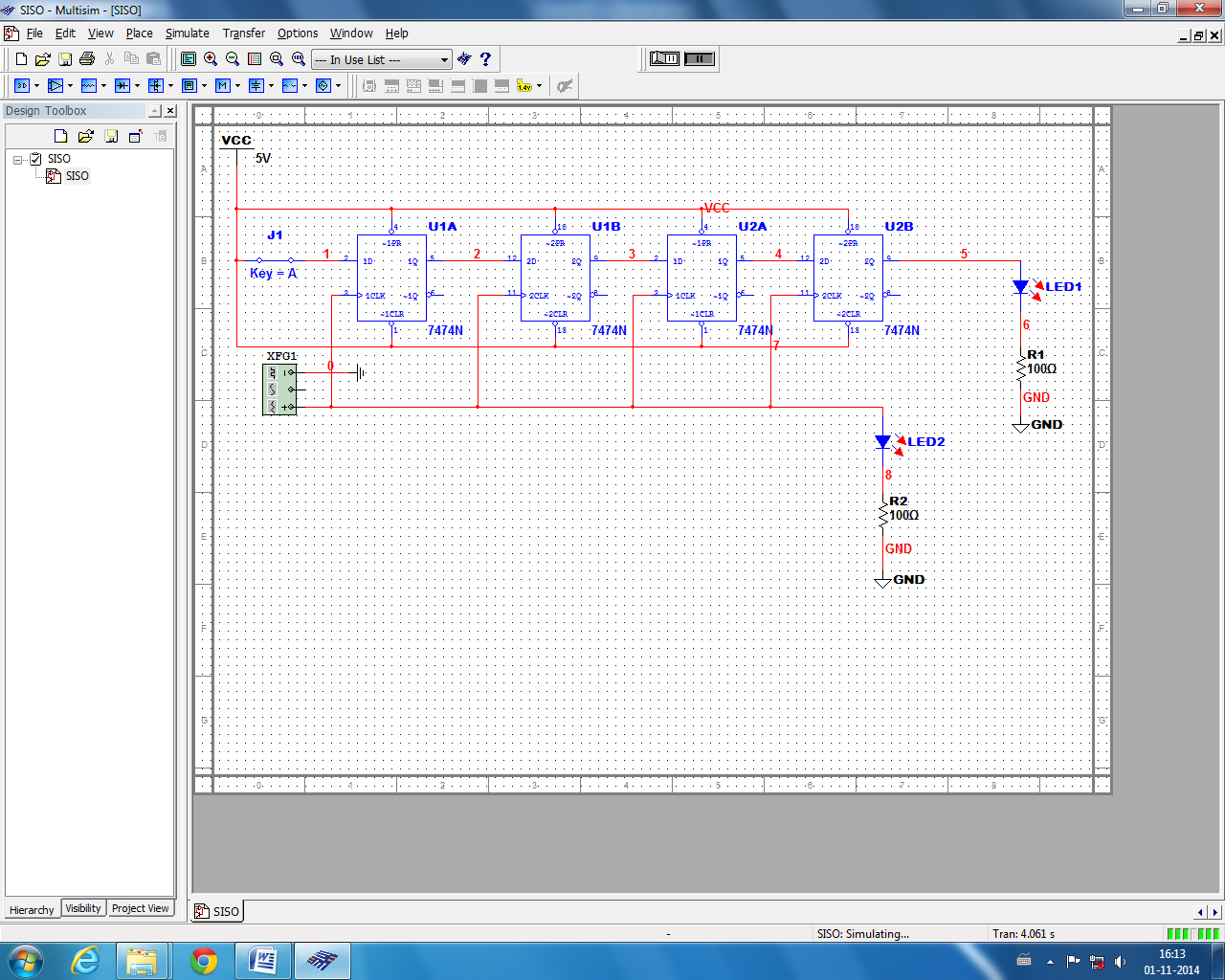


**Experiment: 8**

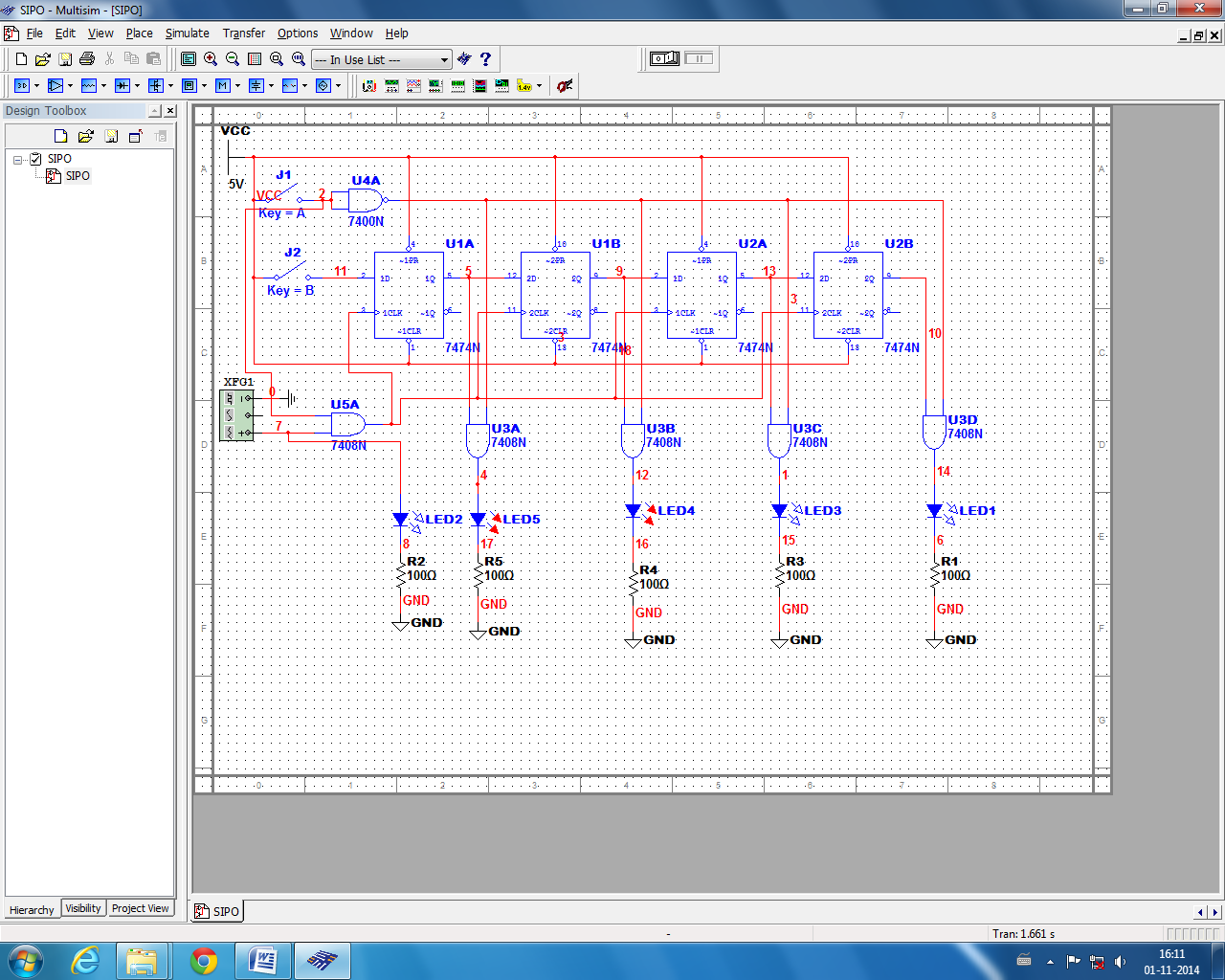
**Aim:**  To design a MOD-5 counter from 1 to 5 states using JK flip flop.



**Experiment: 9**

**Aim:** Design and implement Shift registers (SISO, SIPO, and PIPO) using D flip-flop.

1. SISO: Serially In –Serially Out
2. SIPO : Serially In – Parallelly Out



1. PIPO: Parallelly In – Parallelly Out

